2-PORT Register File
256 WORDS X 24 BITS, MUX 4
SMIC 0.18um G Logic Process

Version 0.2.b

OVERVIEW

The 2-PORT Register File is designed for SMIC's 0.18um CMOS Logic process. The memory is optimized for speed, power and area. It operates at a voltage range of 1.62V to 1.98V and a temperature range of -40^{o} C to 125^{o}C.

Chip enable (CENA,CENB), address (AA[i-1:0],AB[i-1:0]) and data in (DB[n-1:0]) signals are latched on the rising-edge of the clock. When CENA is low, the memory is in read-mode. Data is read from the memory location specified on the address bus AA[i-1:0] and appears on the data output bus QA[n-1:0].When CENB is low, the memory is in write-mode. The word on the data port DB[n-1:0] will be written into the location specified by the address AB[i-1:0] and the data will appear on the output port QA[n-1:0].When CENA is high, port A enters the standby mode. Data outputs remained stable.When CENB is high, port B enters the standby mode. Data stored in the memory is retained, but the new data writes is not allowed.

CONFIGURATION:

PARAMETER	VALUE
Mux	4
Words	256
Bits	24
Width	670.9um
Height	159.945um
Area	107307.100um^{2}

PIN DEFINITION:

PIN	DIRECTION	DEFINITION
AA[7:0]	Input	A Port Address Inputs
AB[7:0]	Input	B Port Address Inputs
DB[23:0]	Input	B Port Data Inputs
CENA	Input	A Port Enable
CENB	Input	B Port Enable
CLKA	Input	A Port Clock Input
CLKB	Input	B Port Clock Input
QA[23:0]	Output	Data Outputs

TIMING:

PARAMETER	DESCRIPTION	FF CORNER 1.98V, -40°C		FF CORNER 1.98V, 0°C		FF CORNER 1.98V, 125°C		SS CORNER 1.62V, -40°C		SS CORNER 1.62V, 125°C		TT CORNER 1.8V, 25°C	
(ns)		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Tcyc	Cycle Time	1.239		1.336		1.600		2.862		3.593		1.931	
Ta	[1]Access Time	0.593		0.639		0.766			2.168		2.722		1.463
Tah	Address Hold	0.333		0.363		0.433		0.612		0.744		0.534	
Tas	Address Setup	0.592		0.617		0.692		1.125		1.293		0.789	
Tch	Cen Hold	0.100		0.100		0.100		0.100		0.100		0.100	
Tcs	Cen Setup	0.460		0.469		0.495		0.603		0.658		0.526	
Tdh	Data Hold	0.114		0.112		0.118		0.185		0.199		0.171	
Tds	Data Setup	0.338		0.389		0.467		0.808		0.977		0.509	
Tclkh	Clock High	0.050		0.060		0.060		0.060		0.080		0.070	
Tclkl	Clock Low	0.200		0.220		0.240		0.210		0.260		0.290	
Tclkr	Clock Rise Skew	1.500		1.500		1.500		3.000		3.000		2.000	
Tcc	Clock Collision	1.239		1.336		1.600		2.862		3.593		1.931	

Timing simulation conditions:

1. Access time = best case for fast corner and worst case for slow/typical corners

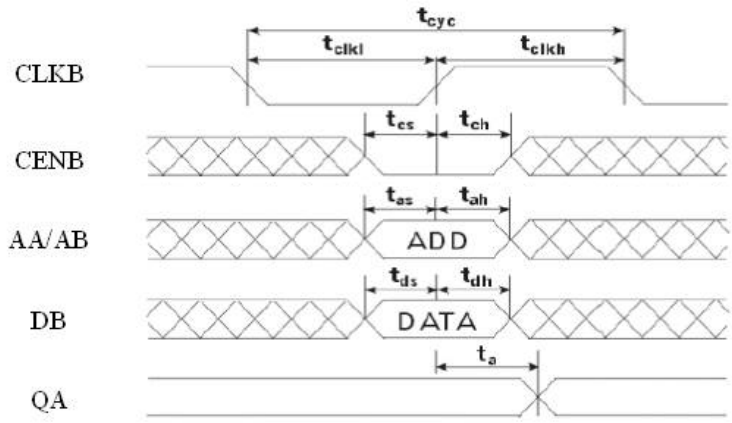
POWER:

PARAMETER	FF CORNER 1.98V, -40°C	FF CORNER 1.98V, 0°C	FF CORNER 1.98V, 125°C	SS CORNER 1.62V, -40°C	SS CORNER 1.62V, 125°C	TT CORNER 1.8V, 25°C
[2]AC Current (uA/MHz)	56.336	51.680	63.136	39.980	20.870	28.554
Read AC Current (uA/MHz)	44.811	42.494	54.901	24.262	18.712	29.519
Write AC Current (uA/MHz)	67.861	60.865	71.372	55.698	23.027	27.589
Standby Power (mW)	0.204525	0.261585	1.085347	0.000570	0.025901	0.049860
[3]Deselect Current (uA/MHz)	14.774	14.211	10.929	6.725	7.823	6.481

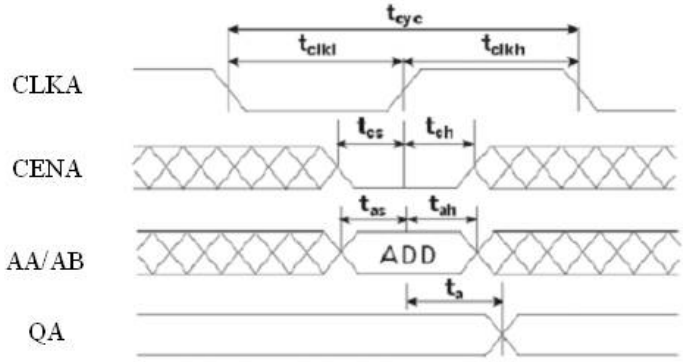
Power simulation conditions:

2. CEN is low, 50% read / 50% write operations, all addresses and 50% of input pins toggle at 1Mhz
3. CEN is high, 50% of input pins toggle at 1Mhz

WRITE CYCLE TIMING:



READ CYCLE TIMING:



Datasheet Revision History

Date	Version	Changes
	null	

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